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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 12/276,344
Filing Date: November 23, 2008
Appellant(s): ALROD ET AL.

Jose M. Nunez
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 9, 2012 appealing from the Office action mailed November 28, 2011.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application: 1-30.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

US-2005/0144357	Sinclair, Alan Welsh	06-2005
US-2006/0039196	Gorobets et al.	02-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sinclair (US 2005/0144357 A1) in view of Gorobets et al. (US 2006/0039196 A1).

Regarding claims **1 and 12**, Sinclair teaches **a method for storing data, the method comprising the steps of**

(a) receiving data to be stored in a memory that includes a plurality of blocks/word-lines [adaptive logical blocks/adaptive logical metablocks, ¶ 0016; and word lines, ¶ 0004]**, wherein each block/word-line from the plurality of blocks has**

at least one metadata value [overhead data that includes parameters relating to the sector data, FIG. 3; and parameters further defined in ¶ 0057-58] **associated with said each block/word-line, said block metadata value being dependent upon a writing time of said each block/word-line** [indications of voltage levels to be used for programming and/or erasing the erase block, ¶ 0058]**; (b) grouping said plurality of blocks/word-lines into block/word-line groups, wherein at least one block/word-line group contains at least two blocks/word-lines** [adaptive logical blocks may be formed so that boundaries between adaptive logical blocks reflect boundaries in the data, ¶ 0017]**.**

Sinclair, however, does not explicitly teach: **(c) associating a respective group metadata value with each block/word-line group; and (d) associating ache group metadata value with each block/word-line in a respective block/word-line group, wherein each block from the plurality of blocks does not store a dedicated copy of said block metadata value, and for each block utilizes the group metadata value instead of the block metadata value.**

On the one hand, Sinclair does teach that adaptive metablocks may be formed according to the data to be stored (in the blocks/word-lines corresponding to the adaptive metablocks) [¶ 0016]. Sinclair further teaches that adaptive logical blocks may be formed so that boundaries between adaptive logical blocks reflect boundaries in the data [¶ 0017]; and finally that the blocks/word-lines that form these adaptive logical blocks and metablocks have overhead data, including parameters such as the voltage levels used for programming and/or erasing these blocks [¶ 0058].

On the other hand, Gorobets discloses that the voltage levels, referred to as threshold levels (V_t), shift as a result of charge disturbing programming, reading or erasing operations performed in the neighboring or other related memory cells, pages or blocks [¶ 0013]. Gorobets further teaches a scrub operation to reduce the corruption of data that happens overtime due to V_t shifting [¶ 0015]. Finally Gorobets discloses that Flash memories place time constraints on reading and other operations [¶ 0024].

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to extend Sinclair method for grouping blocks with common data or similar boundaries, to group blocks that reflect V_t shift as indicted by Gorobets. Forming the adaptive logical groups based on the V_t shift logically groups blocks that potentially need scrubbing, provides a hierarchy that allows for faster scrubbing, since the blocks in need for scrubbing have already been logically grouped. This V_t shift-base hierarchy results in a more efficient scrubbing scheme that can more adequately meet the Flash time constraints as disclosed by Gorobets.

Regarding claims **2 and 13**, the combination Sinclair/Gorobets teaches **the method of claim 1/12, wherein said group metadata value is value selected from a group consisting of: a data age, an optimal-reading threshold-voltage, an optimal-verify threshold-voltage, a number of soft bits read, or data related to error correction** [V_t on Gorobets, and voltage level on Sinclair]**.**

Regarding claims **3 and 14**, the combination Sinclair/Gorobets teaches **the method of claim 1/12, wherein said group metadata value is stored in a block/word-line-group table** [Sinclair further teaches the use of tables to store

information across the adaptive logical blocks, tables having and entry for each logical group; ¶ 0020].

Regarding claim **15**, the combination Sinclair/Gorobets teaches **the method of claim 12, wherein each said word-line is contained in a block/word-line, and wherein at least one block/word-line contains two word-lines belonging to different block/word-line groups** [adaptive logical blocks may be formed so that boundaries between adaptive logical blocks reflect boundaries in the data, ¶ 0017].

Regarding claims **4 and 16**, the combination Sinclair/Gorobets teaches **the method of claim 1/12, wherein said step of grouping is based on a tag that is common to all blocks/word-lines in a block/word-line group** [forming adaptive logical groups with common V_t shift, see discussion for claim 1]**, wherein said tag is associated with an approximate relative time of writing said blocks/word-lines for said block/word-line group** [V_t shifts as a result of charge disturbing programming, Gorobets ¶ 0013, therefore V_t shift is **associate to the time of writing**/programming].

Regarding claims **5 and 17**, the combination Sinclair/Gorobets teaches **the method of claim 4/15, wherein a time since power-up of said memory is divided into time intervals** [timestamp, Gorobets ¶ 0026].

Sinclair/Gorobets, however, do not explicitly teach **wherein blocks/word-lines written during different said time intervals are associated with different tags.**

On the other hand, Gorobets do teaches time-stamping the blocks as they are updated, “controller may timestamp sectors as they are written (for example, by putting

time data in the header/overhead)," to track the order in which sectors in the non-volatile memory array were written [¶ 0198].

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to correlate the timestamp with the V_t shift when forming the adaptive logical blocks, whenever is necessary to track the order in which sectors in the non-volatile memory array were written.

Regarding claims **6 and 18**, the combination Sinclair/Gorobets teaches **the method of claim 5/16, wherein blocks/word-lines written during two different power-up sessions of said memory are associated with different tags** [timestamps saved on non-volatile memory, Gorobets ¶ 0198, can be used to correlated time across **different power-up sessions;** because the memory is non-volatile and therefore suffers little or no data loss across **different power-up sessions**].

Regarding claims **7 and 19**, Sinclair teaches **a method for storing data, the method comprising the steps of: (a) receiving data to be stored in a memory that includes a plurality of blocks/word-lines** [adaptive logical blocks/adaptive logical metablocks, ¶ 0016; and word lines, ¶ 0004]**, wherein each block/word-line from the plurality of blocks has at least one block metadata value** [overhead data that includes parameters relating to the sector data, FIG. 3; and parameters further defined in ¶ 0057-58] **associated with said each block/word-line, said block metadata value being dependent upon a writing time of said each block/word-line** [indications of voltage levels to be used for programming and/or erasing the erase block, ¶ 0058]**; (b) grouping said plurality of blocks/word-lines into block/word-line groups, wherein**

at least one said block/word-line group contains at least two blocks/word-lines [adaptive logical blocks may be formed so that boundaries between adaptive logical blocks reflect boundaries in the data, ¶ 0017]**.**

Sinclair, however, does not explicitly teaches: **(c) associating a sequential tag with each block/word-line group, wherein blocks in a first block/word-line group having a previous sequential tag are written before blocks in a second block/word-line group having a subsequent sequential tag; and (d) associating a group metadata value with each respective sequential tag, wherein each block from the plurality of blocks does not store a dedicated copy of said block metadata value, and each block utilized the group metadata value instead of the block metadata value.**

On the one hand, Sinclair does teach that adaptive metablocks may be formed according to the data to be stored (in the blocks/word-lines corresponding to the adaptive metablocks), and that logical groups are further formed from logically sequential sectors [¶ 0016]. Sinclair further teaches that adaptive logical blocks may be formed so that boundaries between adaptive logical blocks reflect boundaries in the data [¶ 0017]; and finally that the blocks/word-lines that form these adaptive logical blocks and metablocks have overhead data, including parameters such as the voltage levels used for programming and/or erasing these blocks [¶ 0058].

On the other hand, Gorobets do teaches time-stamping the blocks as they are updated, “controller may timestamp sectors as they are written (for example, by putting

time data in the header/overhead)," to track the order in which sectors in the non-volatile memory array were written [¶ 0198].

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to include the timestamp information in along with the other parameters in Sinclair's overhead data; to track the order in which sectors in the non-volatile memory array were written.

Regarding claims **8 and 20**, the combination Sinclair/Gorobets teaches **the method of claim 7/19, wherein said at least one metadata value is selected from a group consisting of: a data age, an optimal-reading threshold-voltage, an optimal-verify threshold-voltage, a number of soft bits read, or data related to error correction** [data age can be determined by the timestamp]**.**

Regarding claims **9 and 21**, the combination Sinclair/Gorobets teaches **the method of claim 7/19, wherein said group metadata value is stored in a block/word-line-group table** [Sinclair further teaches the use of tables to store information across the adaptive logical blocks, tables having and entry for each logical group; ¶ 0020].

Regarding claim **10**, the combination Sinclair/Gorobets teaches **the method of claim 7, wherein a time since power-up of said memory is divided into time intervals, and wherein blocks written during different said time intervals are associated with different tags** [timestamps are indicative of time intervals]**.**

Regarding claim **11**, the combination Sinclair/Gorobets teaches **the method of claim 10, wherein said blocks written during two different power-up sessions of**

said memory are associated with different tags [timestamps saved on non-volatile memory, Gorobets ¶ 0198, can be used to correlated time across **different power-up sessions;** because the memory is non-volatile and therefore suffers little or no data loss across **different power-up sessions**].

Regarding claim **22**, the combination Sinclair/Gorobets teaches **the method of claim 19, wherein each said word-line is contained in a block, and wherein at least one block contains two word-lines belonging to different word-line groups** [Gorobets ¶ 0058, and Sinclair ¶ 0004]**.**

Regarding claims **23 and 25**, these claims are directed to **a controller** [Sinclair FIG. 1A, Gorobets FIG. 1A] for performing the steps as outlined in claims 1 and 12; and are therefore rejected under the same ground.

Regarding claims **24 and 26**, these claims are directed to **a controller** [Sinclair FIG. 1A, Gorobets FIG. 1A] for performing the steps as outlined in claims 7 and 19; and are therefore rejected under the same ground.

Regarding claims **27 and 29**, these claims are directed toward **a computer-readable non-transitory storage medium having computer-readable code embodied therein**, to implement the methods as outlined in claims 1 and 12; and are therefore rejected under the same ground.

Regarding claims **28 and 30**, these claims are directed toward **a computer-readable non-transitory storage medium having computer-readable code embodied therein**, to implement the methods as outlined in claims 7 and 19; and are therefore rejected under the same ground.

(10) Response to Argument

Appellants' arguments have been fully and carefully considered, with the Examiner's response set forth below.

1. Answer to Argument on rejection of Claims 1, 7, 12, 19, and 23-30; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

i. Appellant initially argues that "the prior art does not teach that said block metadata value [is] dependent upon a writing time of said each block" [Appeal Brief p.11, section IV.A.1.i]. However, the body of this section, and evidence for the particular argument, relates to what the appellant calls a "lack of consistency" on the office action. In particular the appellant indicates that "the Examiner believes that 'adaptive logical blocks' teaches both a 'block' and a 'block group'", and therefore "the Examiner's rejection lacks rational underpinnings because the rejection lacks consistency" [Appeal Brief p.12, 4th paragraph]. The examiner respectfully disagrees.

There seems to be a confusion regarding the mapping of the prior art elements to the claim limitations. By addressing the different appellant arguments on the previous Office Actions, the examiner has tried to clear this confusion. To aid on clearing any confusion the examiner presents Figure 1 and Figure 2 below.

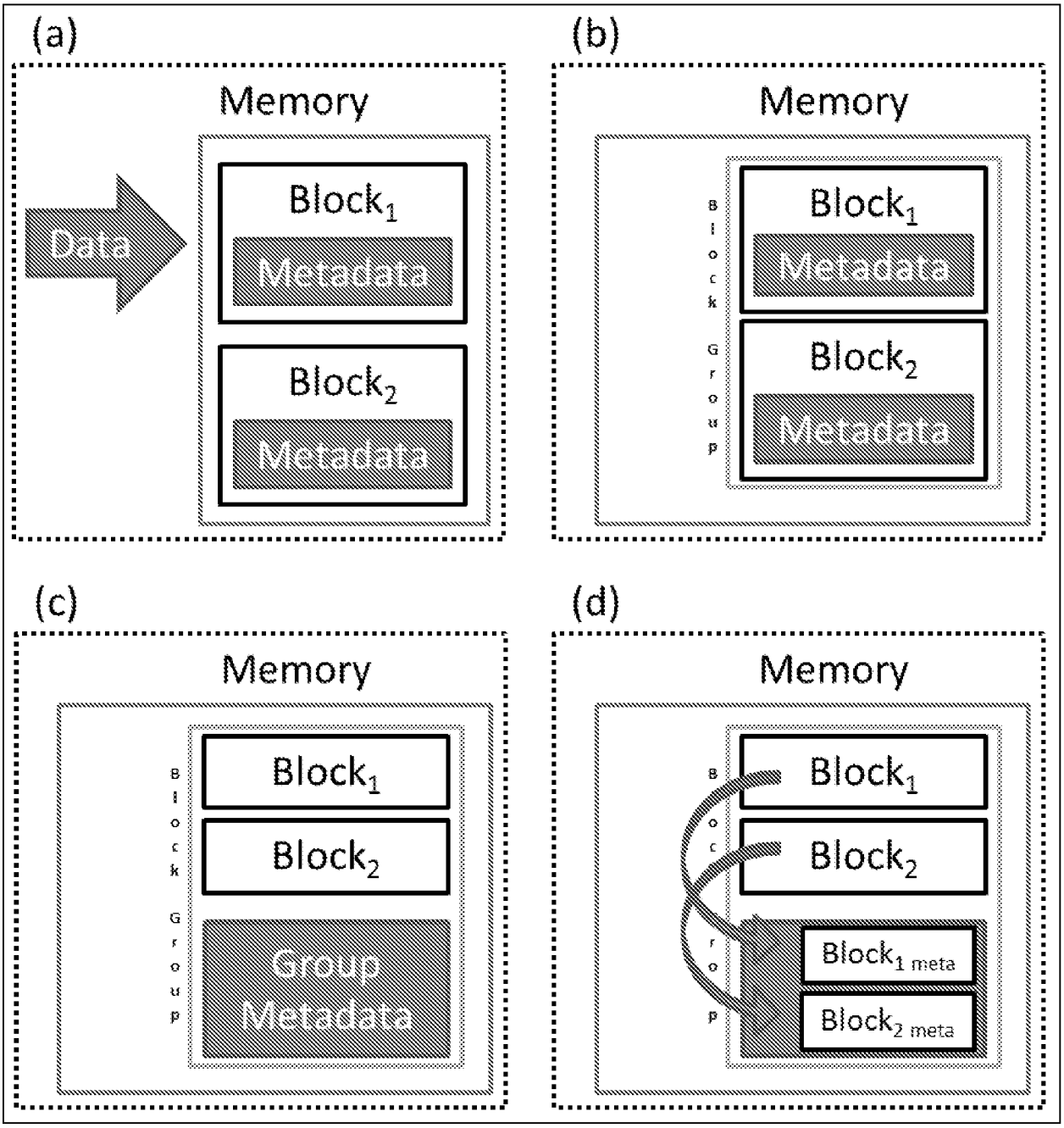

Figure 1

Figure 1 shows a graphical representation of a broad reasonable interpretation of the limitations on claim 1. In detail, Figure 1(a) shows receiving data to be stored in a

memory that includes a plurality of blocks, wherein each block from the plurality of blocks has at least one block metadata value associated with said each block, said block metadata value being dependent upon a writing time of said each block. Figure 1(b) represents grouping said plurality of blocks into block groups, wherein at least one block group contains at least two blocks. Figure 1(c) shows associating a group metadata value with each block group; and Figure 1(d) represents associating each group metadata value with each block in a respective block group, wherein each block from the plurality of blocks does not store a dedicated copy of said block metadata value, and each block utilizes the group metadata value instead of the block metadata value. Similarly, Figure 2 shows relevant elements of the Sinclair prior art.

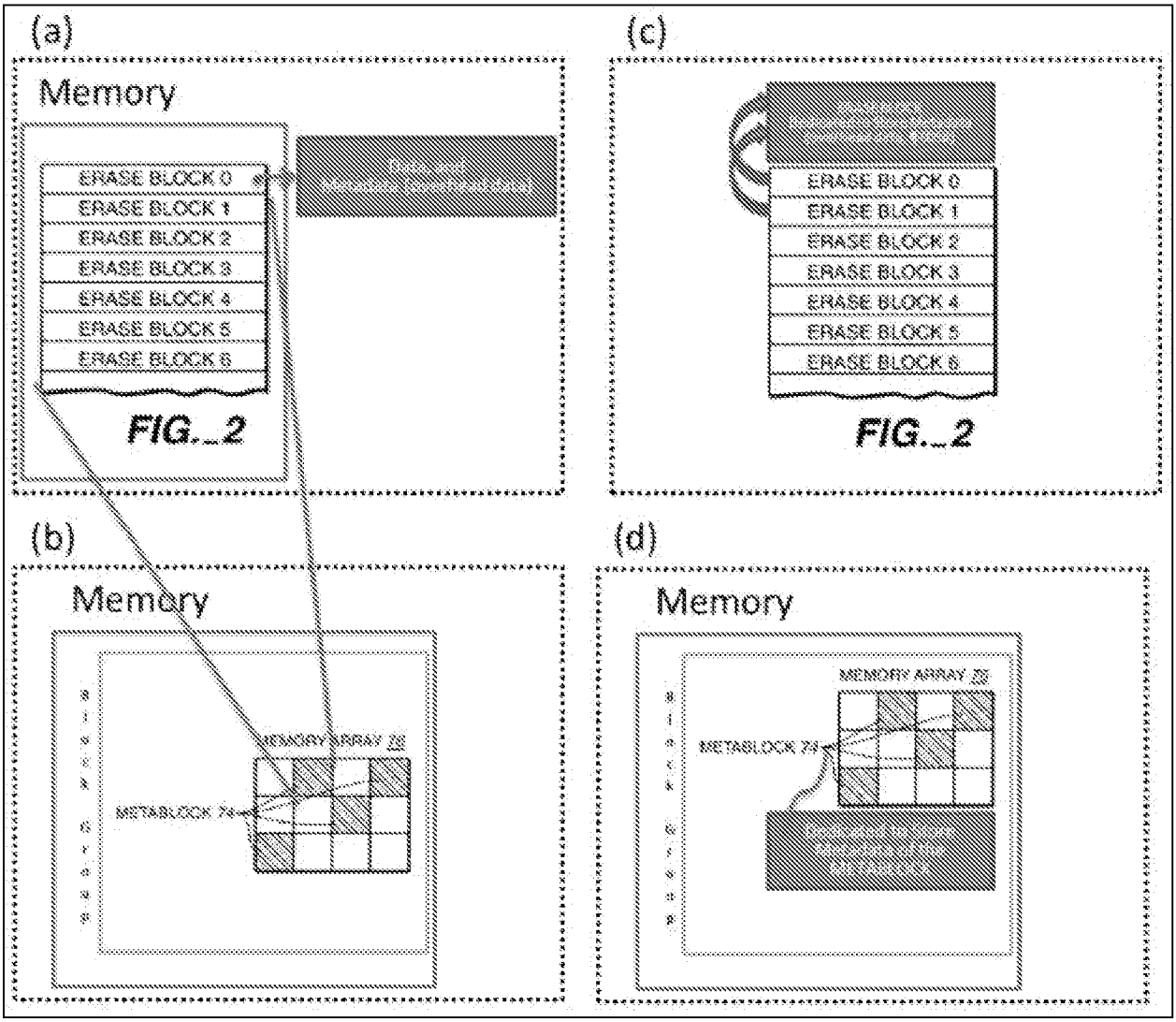

Figure 2

In particular, Figure 2(a) illustrates a portion of a memory array wherein **memory cells** are **grouped** into **erase blocks** [¶ 0055 and FIG. 2 on Sinclair]. Figure 2(b) shows the relationship between metablocks and erase block. In particular, Sinclair discloses that in order to increase the degree of parallelism of operation, **erase blocks** within different planes are **logically linked** (i.e. grouped) to form **metablocks** [¶ 0063 and FIG. 6 on Sinclair; and Figures 2(a) and 2(b) above]. Sinclair further discloses that,

while the size of the individual memory cell erase blocks may vary, one commercially practiced form includes a **single sector of data** in an individual **erase block**; where the **contents** of such a sector includes **user data, parameters, and any other overhead data** [¶ 0056 and FIG. 3 on Sinclair]. What's more, Sinclair discloses that some or **all of the overhead data** can be **stored** in **erase blocks dedicated to such a function**, rather than in the erase block containing the user data or to which the overhead data pertains [¶ 0058 on Sinclair].Figure 2(c) shows such an erase block dedicated to store the overhead data.

Therefore, and extrapolating from Sinclair's teachings above, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to extend the block organization disclosed for erase blocks to metablocks, where some or all of the overhead data can be stored in **metablocks dedicated to such a function**, rather than in the erase block containing the user data or to which the overhead data pertains. The modification would be obvious because one of the ordinary skills in the art would want to increase the degree of parallel operation for overhead access as well as for user data access [¶ 0063]. This is consistent with what was previously presented on the Office Action dated November 28, 2011; 2nd paragraph page 3.

Finally, claim 1 recites "said block metadata value being dependent upon a writing time of said each block". With respect to this particular limitation, on the one hand, Sinclair discloses that the overhead data parameters may include a quantity related to the number of program/erase cycles experienced by the erase block. When this experience quantity is used in a wear leveling algorithm, logical block addresses are

regularly re-mapped to different physical block addresses in order to even out the usage (wear) of all the erase blocks. Another use of the experience quantity is to **change voltages** and other **parameters of programming**, reading and/or erasing as a function of the number of cycles experienced by different erase blocks [¶ 0057].

On the other hand, Gorobets discloses that the **voltage levels**, referred to as threshold levels (V_t), shift as a result of charge disturbing **programming**, reading or erasing operations performed in the neighboring or other related memory cells, pages or blocks [¶ 0013]. Gorobets further teaches a scrub operation to reduce the corruption of data that happens overtime due to V_t shifting [¶ 0015]. Moreover, Gorobets discloses that Flash memories place time constraints on reading and other operations [¶ 0024].

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to extend Sinclair method to include Gorobets' threshold levels (V_t), a quantity that shift as a result of charge disturbing **programming** in the neighboring or other related memory cells, pages or blocks (i.e. used at writing time of each block and that changes with time as operations on neighboring or other related memory cells, pages or blocks are performed) [¶ 0013].

ii. Appellant further argues that “the prior art does not teach associating a group metadata value with each block group” [Appeal Brief p.13, section IV.A.1.ii]. In particular the Appellant discloses that "it may appear that the Examiner means that a metablock teaches a block group, and that an erase block teaches the claimed block" [Appeal Brief p.14, fourth paragraph]. The examiner respectfully disagrees.

From the body of the argument, it seems that the argument regarding the prior art not teaching associating a group metadata value with each block group, stems from the confusion regarding the mapping of the prior art elements to the claim limitations. The previous discussion, and in particular the included Figures 1 and 2, should clarify, how the prior art teaches associating **each group metadata value** with **each block** in a respective block group.

iii. Appellant further argues that “the prior art does not teach that each block from the plurality of blocks does not store a dedicated copy of said block metadata value and each block utilizes the group metadata value instead of the block metadata value” [Appeal Brief p.17, section IV.A.1.iii]. Similarly to the previous arguments, the appellant indicates that "it appears that here, the Examiner believes that a block is taught by a memory cell and that the block group is taught by an erase block", and that since “Sinclair teaches values associated with the erase block, Sinclair does not teach values associated with the memory cells, only with the erase blocks”, “the prior art does not teach the aforementioned feature” [Appeal Brief p.18, second to last paragraph]. The examiner respectfully disagrees.

As pointed out earlier, Sinclair discloses that, while the size of the individual memory cell erase blocks may vary, one commercially practiced form includes a single sector of data in an individual **erase block**; where the **contents** of such a sector includes **user data, parameters, and any other overhead data** [¶ 0056 and FIG. 3 on Sinclair]. Sinclair further discloses that some or **all of the overhead data** can be **stored** in **erase blocks dedicated to such a function**, rather than in the erase block

containing the user data or to which the overhead data pertains [¶ 0058 on Sinclair]. Therefore Sinclair teaches associating each group metadata value (overhead) with each block (erase block) in a respective block group (dedicated metablock, Figure 2(d) above).

2. Answer to Argument on rejection of Claims 4 and 16; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that “the prior art does not teach that said step of grouping is based on a tag that is common to all blocks in a block group, wherein said tag is associated with an approximate relative time for writing said blocks of said block group” [Appeal Brief p.18, section IV.A.2.i]. In particular the appellant points out that " the Vt shift is associated with operations performed on another group of memory cells, and not on the "time for writing said blocks" as claimed". The examiner respectfully disagrees.

Claims **4 and 16** recite “wherein said tag is associated with an **approximate relative time** for writing said blocks”. As previously indicated Gorobets' threshold level (V_t), is quantity that shift as a result of charge disturbing **programming** in the neighboring or other related memory cells, pages or blocks (i.e. used at writing time of each block and that changes with time as operations on neighboring or other related memory cells, pages or blocks are performed). Therefore V_t is clearly associated with an **approximate relative time** for writing said blocks.

3. Answer to Argument on rejection of Claims 5, 10 and 17; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that "the prior art does not teach that a time since power-up of said memory is divided into time intervals, and wherein blocks written during different time intervals are associated with different tags" [Appeal Brief p.19, section IV.A.3.i]. In particular, the Appellant indicates that "the timestamp does not teach a time interval, and the prior art does not teach the aforementioned feature" [Appeal Brief p.20, first paragraph]. The examiner respectfully disagrees.

Claim 4 recites "wherein a time since power-up is divided into time intervals". In computers time is divided into CPU cycles, i.e. the cycle is the smallest time interval in a computer system. Gorobets' timestamp is an indication of the number of cycles ["the memory controller may timestamp sectors as they are written (for example, by putting time data in the header)", ¶ 0198]. Gorobets' further teaches using this timestamp to control the scrubbing function on blocks of data ["the relative freshness of **various units of data** may be maintained, for example, with timestamps stored with the units of data, such as in part of overhead data of the blocks", ¶ 0064]. Therefore, blocks written during different time intervals (i.e. at different clock cycles) are associated with different tags (i.e. have different timestamps).

4. Answer to Argument on rejection of Claims 2, 8, 13, and 20; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that "the prior art does not teach the features of these claims" [Appeal Brief p.20, section IV.A.4.i]. However, no particular evidence is presented regarding how the prior art does not teach the limitations of these claims.

Therefore, the examiner maintains that the prior art of record does teach the particular limitations; and the claims remain rejected in view the prior art.

Answer to Argument on rejection of Claims 3, 9, 14, and 21; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that "the prior art does not teach the features of these claims" [Appeal Brief p.20, section IV.A.5.i]. However, no particular evidence is presented regarding how the prior art does not teach the limitations of these claims.

Therefore, the examiner maintains that the prior art of record does teach the particular limitations; and the claims remain rejected in view the prior art.

5. Answer to Argument on rejection of Claims 6, 11, and 18; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that "the prior art does not teach the features of these claims" [Appeal Brief p.21, section IV.A.6.i]. However, no particular evidence is presented regarding how the prior art does not teach the limitations of these claims.

Therefore, the examiner maintains that the prior art of record does teach the particular limitations; and the claims remain rejected in view the prior art.

Answer to Argument on rejection of Claims 15 and 22; under 35 U.S.C. § 103(a) over Sinclair in view of Gorobets.

Appellant initially argues that "the prior art does not teach the features of these claims" [Appeal Brief p.21, section IV.A.7.i]. However, no particular evidence is presented regarding how the prior art does not teach the limitations of these claims.

Therefore, the examiner maintains that the prior art of record does teach the particular limitations; and the claims remain rejected in view the prior art.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/RAMON A MERCADO/

Examiner, Art Unit 2186

Conferees:

/Charles Rones/

Supervisory Patent Examiner, Art Unit 2186

/Manorama Padmanabhan/

Supervisory Patent Examiner, Art Unit 2188