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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/322,293	05/23/2023	Yusuke YAMAMOTO	8323-0058	4056

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EXAMINER	
TRAN, DZUNG	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
12/16/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 18/322,293	Applicant(s) YAMAMOTO, Yusuke	
	Examiner DZUNG T TRAN	Art Unit 2893	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 09/30/2025.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-8 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-8 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 05/23/2023 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Status of the Claims

1. Applicant's election, without traverse, of Specie I (Fig. 4A), claims 1-8 in the reply filed on September 30th, 2025 is acknowledged. Claims 1-8 are pending.

Action on merits of Group I, Species 1, claims 1-5 and 21-24 follows.

Priority

2. Receipt is acknowledged of certified copies of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on May 23rd, 2023 has been considered by the examiner.

Drawings

4. The drawings filed on 05/23/2023 are acceptable.

Specification

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action: substrate

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

7. Claims 1 and 6-8 are rejected under 35 U.S.C. 103 as being unpatentable over Sekine (US 2015/0123119, hereinafter as Seki '119) in view of Miyamoto (US 2020/0052083, hereinafter as Miya '083).

Regarding Claim 1, Seki '119 teaches an image sensor (900; [0078]), comprising:

pixels arrayed (Fig. 9, (910); [0078]) on a substrate (200; [0063]); and

a data line (D1-D4; [0078]) that transmits a signal read from each of the pixels, wherein the pixel includes: a photodetector (912; [0078]); and an N-type switch thin film transistor (911;

[0078]) between the photodetector (912) and the data line (D1-D4), wherein the switch thin film transistor includes: an oxide semiconductor part (130; [0047]); a gate electrode (110; [0047]); a drain electrode (140; [0047]) towards the data line; and a source electrode (145; [0047]) towards the photodetector (see Fig. 1).

Thus, Seki '119 is shown to teach all the features of the claim with the exception of explicitly the features: "an overlap region where the gate electrode and the drain electrode overlap in a plan view is smaller than an overlap region where the gate electrode and the source electrode overlap in a plan view".

Miya '083 teaches an overlap region where the gate electrode (Fig. 2B, (3); [0050]) and the drain electrode (9; [0050]) overlap in a plan view is smaller than an overlap region where the gate electrode (3) and the source electrode (8; [0050]) overlap in a plan view (see Fig. 2B).

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Seki '119 by having an overlap region where the gate electrode and the drain electrode overlap in a plan view is smaller than an overlap region where the gate electrode and the source electrode overlap in a plan view for the purpose of reducing the size of the TFT while securing desired TFT characteristics (see para. [0025) as suggested by Miya '083.

Further, it has been held to be within the general skill of a worker in the art to select a n-type thin film transistor on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. (see para. [0071] of US 2021/0174051 as evidence). A person of ordinary skills in the art is motivated to have a n-type thin film transistor the switching TFT when this improves the performance of the image sensor device.

Regarding Claim 6, Seki '119 teaches the switch thin film transistor (911) is connected between a cathode terminal of the photodetector (912) and the data line (D1) (see Fig. 9).

Regarding Claim 7, Seki '119 teaches the gate electrode (Fig. 6, (110); [0047]) is positioned between the oxide semiconductor part (130; [0044]) and the substrate (200) (see Fig. 6).

FIG. 9

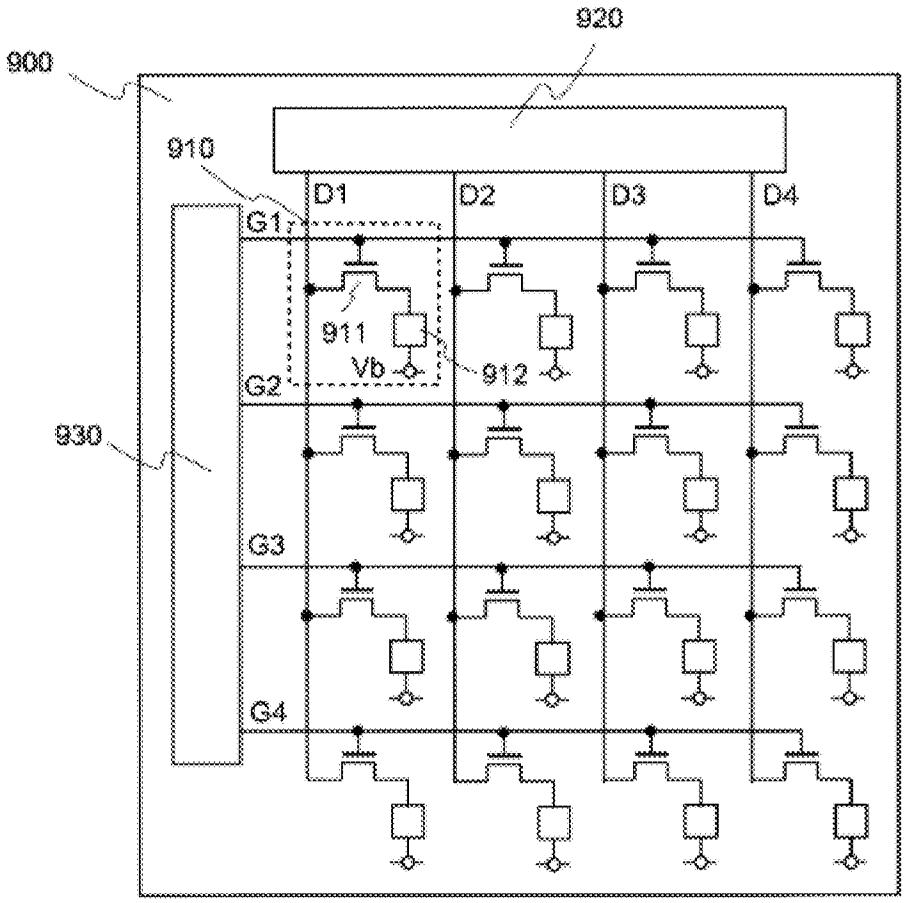

Fig. 9 (Seki '119)

Regarding Claim 8, Seki '119 teaches a region of the oxide semiconductor part (130) between the source electrode and the drain electrode is covered by an etch stop (135; [0044]). Examiner considers the channel protection film (135; [0047]) is the etch stop.

8. Claims 2-5 are rejected under 35 U.S.C. 103 as being unpatentable over Seki '119 and Miya '083 as applied to claim 1 above, and further in view of Chiu (US 2006/0170048, hereinafter as Chiu '048).

Regarding Claim 2, Seki '119 and Miya '083 are shown to teach all the features of the claim with the exception of explicitly the features: "the gate electrode does not overlap the drain electrode in a plan view, and wherein a portion of the gate electrode overlaps the source electrode in a plan view".

Chiu '048 teaches the gate electrode (Fig. 2A, (302); [0027]) does not overlap the drain electrode (Fig. 2A, (324); [0027]) in a plan view, and wherein a portion of the gate electrode (Fig. 2A, (302); [0027]) overlaps the source electrode (Fig. 2A, (322); [0027]) in a plan view.

Thus, it would have been obvious to a person of ordinary skill in the art before the effective filing date of the invention to modify Seki '119 and Miya '083 by having the gate electrode does not overlap the drain electrode in a plan view, and wherein a portion of the gate electrode overlaps the source electrode in a plan view in order to reduce Cgd capacitance (see para. [0027]) for improving the performance of the display device (see para. [0004]-[0005]) as suggested by Chiu '048.

Regarding Claim 3, Chiu '048 teaches a drain electrode side edge of the gate electrode (302) is in a region between a source electrode side edge of the drain electrode (324) and a drain electrode side edge of the source electrode (322) (see Fig. 2A).

Further, it has been held to be within the general skill of a worker in the art to select a drain electrode side edge of the gate electrode is in a region between a source electrode side edge

of the drain electrode and a drain electrode side edge of the source electrode on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. A person of ordinary skills in the art is motivated to have a drain electrode side edge of the gate electrode is in a region between a source electrode side edge of the drain electrode and a drain electrode side edge of the source electrode when this improves the performance of the image sensor device.

Regarding Claim 4, Chiu '048 teaches a drain electrode side edge of the gate electrode (302) matches a drain electrode side edge of the source electrode (322) (see Fig. 3L).

Further, it has been held to be within the general skill of a worker in the art to select a drain electrode side edge of the gate electrode matches a drain electrode side edge of the source electrode on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416. A person of ordinary skills in the art is motivated to have a drain electrode side edge of the gate electrode matches a drain electrode side edge of the source electrode when this improves the performance of the image sensor device.

Regarding Claim 5, Chiu '048 teaches the drain electrode side edge of the gate electrode (302) is a straight line in a channel width direction of the oxide semiconductor part, and wherein the drain electrode-side edge of the source electrode (322) is a straight line in the channel width direction of the oxide semiconductor part (see Fig. 2A)

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to semiconductor devices:

Lee et al. (US 2020/0280664 A1)

Sekine (US 2018/0315792 A1)

Rhee et al. (US 2014/0097437 A1)

Ie et al. (US 2011/0046341 A1)

Kang et al. (US 2010/0133539 A1)

10. For applicant's benefit portions of the cited reference(s) have been cited to aid in the review of the rejection(s). While every attempt has been made to be thorough and consistent within the rejection it is noted that the *PRIOR ART MUST BE CONSIDERED IN ITS ENTIRETY, INCLUDING DISCLOSURES THAT TEACH AWAY FROM THE CLAIMS.* See MPEP 2141.02 VI.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DZUNG T TRAN whose telephone number is (571) 270-3911. The examiner can normally be reached on M-F 8 AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DZUNG TRAN/
Primary Examiner, Art Unit 2893