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EXAMINER	
COUGHLIN, ANDREW J	

ART UNIT	PAPER NUMBER
3992	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 18/375,197	Applicant(s) Delacruz et al.	
	Examiner ANDREW J COUGHLIN	Art Unit 3992	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 29 September 2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-50 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-50 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 29 September 2023 is/are: a)☐ accepted or b)☑ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

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B. Claims 3, 9, 30, 31, 45, 46, 50 are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra") and US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano") as applied to claims 1, 7, 24, 39, and 49 above, and further in view of US 8,399,974 B1 to Huneke ("Huneke") 31
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E. Claims 16, 17, 32, 33, 38, 47 and 48 are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra") and US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano") as applied to claims 6 and 34 above, and further in view of US Pub. No. 2008/0157393 A1 to Kodama et al. ("Kodama") 35

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I. Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

II. Priority

Applicant filed the instant reissue application 18/375,197 ("'197 Reissue Application") on 09/29/2023 for U.S. Application No. 16/533,003 ("'003 Application"), filed 08/06/2019, now U.S. Patent No. 11,139,283 ("'283 Patent"), issued 10/05/2021, which claims domestic priority to Provisional Application No. 62/784,426 ("'426 Prov Application"), filed 12/22/2018.

Thus, the Examiner concludes that for examination purposes the instant '197 Reissue Application claims a priority date of 12/22/2018.

III. Pertinent Prosecution History

As set forth *supra*, Applicant filed the application for the instant '197 Reissue Application on 09/29/2023. The Examiner finds that the instant '197 Reissue Application included a preliminary amendment ("09/29/2023 Preliminary Amendment") to the claims ("09/29/2023 Claim Amendment"). The 09/29/2023 Claim Amendment includes an amendment: Adding new claims 24-50.

IV. Claim Status

The Examiner finds that the claim status in the instant '811 Reissue Application is as follows:

Claim(s) 1-23 (Original)

Claim(s) 24-50 (New)

Thus, the Examiner concludes that claims 1-50 are pending in the instant '197 Reissue Application. Claims 1-50 are examined ("Examined Claims").

V. Reissue Requirements

For reissue applications filed before September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the law and rules in effect on September 15, 2012. Where specifically designated, these are "pre-AIA" provisions.

For reissue applications filed on or after September 16, 2012, all references to 35 U.S.C. 251 and 37 CFR 1.172, 1.175, and 3.73 are to the current provisions.

The Examiner notes that Amendment practice for Reissue Applications is NOT the same as for non-provisional applications. See MPEP §§ 1413 and 1453. Reissue application amendments must comply with 37 CFR 1.173, while non-provisional application amendments must comply with 37 CFR 1.121. Particularly,

Manner of making amendments under 37 CFR 1.173:

All markings (underlining and bracketing) are made ***relative to the original patent text***, 37 CFR 1.173(g) (and **not** relative to the prior amendment).

For amendments to the abstract, specification and claims, the deleted matter must be enclosed in brackets, and the added matter must be underlined. See 37 CFR 1.173(d).

For amendments to the drawings, any changes to a patent drawing must be submitted as a replacement sheet of drawings which shall be an attachment to the amendment document. Any replacement sheet of drawings must be in compliance with § 1.84 *and* shall include all of the figures appearing on the original version of the sheet, even if only one figure is amended. Amended figures ***must be*** identified as "Amended," and any added figure must be identified as "New." In the event that a figure is canceled, the figure must be surrounded by brackets and identified as "Canceled." ***All changes to the drawing(s) shall be explained, in detail, beginning on a separate sheet accompanying the papers including the amendment to the drawings***. See 37 CFR 1.173(d)(3).

The Examiner further notes that **all amendments** to the instant '197 Reissue Application **must comply with 37 CFR 1.173(b)-(g)**.

VI. Reissue Oath/Declaration

The Examiner finds that the Declaration filed by Applicant on 9/29/2023 ("9/29/2023 Oath/Declaration") is defective.

A proper error statement must identify a single word, phrase, or expression in the specification or in an original claim in the underlying patent, *i.e.*, the '283 Patent, and how it renders the original patent wholly or partly inoperative or invalid. (See MPEP §1414(II)).

The 9/29/2023 Oath/Declaration is defective because it does not specifically say that the errors would render the original patent wholly or partly inoperative or invalid.

Thus, Applicant is required to provide a new Oath/Declaration with a statement of error with a statement similar to "[W]ithout correcting (*insert 'error'*), original patent claim (*insert 'claim number(s)'*) was unduly narrow."

VII. Drawing Objections

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

The drawings are objected to for the following reasons:

Claims 32, 33, 47 and 48 are embodiments in which the memory device is a volatile memory device or a DRAM device. Therefore, the volatile memory device of DRAM device must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.173(b)(3), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.173(b)(1) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure of an amended drawing should be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be surrounded by brackets and identified as "Canceled," and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.173(b)(3). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

VIII. Specification Objections

The disclosure is objected to because of the following informalities:

In col. 12, ln. 65, change "Fig. 49" to - - Fig. 9 - -.

In col. 13, ln. 7, change "Fig. 49" to - - Fig. 9 - -.

In col. 13, ln. 21, change "Fig. 49" to - - Fig. 9 - -.

In col. 13, ln. 38, change "Fig. 49" to - - Fig. 9 - -.

Appropriate correction is required.

IX. Claim Interpretation

During examination, claims are given the broadest reasonable interpretation consistent with the specification and limitations in the specification are not read into the claims. See MPEP § 2111, MPEP § 2111.01 and *In re Yamamoto et al.*, 222 USPQ 934 (Fed. Cir. 1984). Under a broadest reasonable interpretation, words of the claim must be given their plain meaning, unless such meaning is inconsistent with the specification. See MPEP § 2111.01(I). It is further noted it is improper to import claim limitations from the specification, *i.e.*, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment. See MPEP § 2111.01(II). Therefore, unless one of the exceptions applies below, Examiners will interpret the limitations of the pending and examined claims using the broadest reasonable interpretation ("BRI").

A. Lexicographic Definitions

A first exception to the prohibition of reading limitations from the specification into the claims is when the Applicant for patent has provided a lexicographic definition for the term. See MPEP § 2111.01(IV). Following an independent review of the claims in view of the specification herein, Examiners find that Applicant has not provided any lexicographic definitions related to claim terms with any reasonable clarity, deliberateness and precision.

B. 35 U.S.C § 112 6th Paragraph

Additionally, the Examiner finds that because the Examined Claims do not recite "step," "means" or a claim term used as a substitution for "means" (*i.e.*, a generic placeholder for "means"), the Examined Claims fail Prong (A) as set forth in MPEP §2181. Because the Examined Claims fail Prong (A) as set forth in MPEP §2181 I., the Examiner concludes that all Examined Claims do not invoke 35 U.S.C. §112, 6th paragraph. See also *Ex parte Miyazaki*, 89 USPQ2d 1207, 1215-16 (B.P.A.I. 2008)(precedential).

X. Claim Rejections – 35 U.S.C. § 112

A. 35 U.S.C. 112(b) or pre-AIA 35 U.S.C. 112, second paragraph

The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

> The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 18, 21, and 22 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 18 recites the limitation "wherein the terminals at the second surface of the microelectronic package" in ln. 2-3. There is insufficient antecedent basis for this limitation in the claim. Claim 18 is dependent on claim 1 in which the “second surface” is introduced but that applies to the substrate within the microelectronic package and not necessarily a surface of the entirety of the microelectronic package. The word “terminals” is never properly introduced in claims 1 or 18. For the purpose of examination the Examiner will interpret the claim as though the problematic limitation reads - - wherein terminals at the second surface of the substrate - -.

Claim 21 recites the limitation "**the** front surfaces" in ln. 13. There is insufficient antecedent basis for this limitation in the claim.

For the purpose of examination the Examiner will interpret the claim as though the problematic limitation reads - - front surfaces - -. Eliminating the word "the" is a sufficient correction.

Claim 21 recites "a plurality of microelectronic elements" in line 4,and then also recites the limitation "the microelectronic elements." Later, "the plurality of microelectronic elements in lines 7 and 8 appears before once again referencing "the microelectronic elements" a few more times for the remainder of the claim. It is unclear whether "the microelectronic elements are the same as the "plurality of microelectronic elements" or just a subset thereof.

For the purpose of examination, the Examiner will interpret each occurrence of "the microelectronic elements" to be - - the plurality of microelectronic elements - -.

Claim 22 recites the limitation "microelectronics." There is insufficient antecedent basis for this limitation in the claim. For the purpose of examination the Examiner will interpret the claim as though the problematic limitation reads - - microelectronic elements in the plurality of microelectronic elements- -.

The Examiner finds that because claims 18, 21, and 22 are indefinite under 35 U.S.C. §112 second paragraph as outlined above, it is impossible to properly construe claim scope at this time. See *e.g. Honeywell International Inc. v. ITC*, 68 USPQ2d 1023, 1030 (Fed. Cir. 2003) ("Because the claims are indefinite, the claims, by definition, cannot be construed."). However, in accordance with MPEP § 2173.06 and the USPTO's policy of trying to advance prosecution by providing art rejections even though these claims are indefinite, the claims are construed and the art is applied as much as practically possible.

XI. Claim Rejections – 35 U.S.C. § 251

A. Original Patent Requirement

Claims 24-50 are rejected under 35 U.S.C. 251 as being in violation of the original patent requirement.

Section 251 requires that reissue is for "the invention disclosed in the original patent." In order to satisfy the original patent requirement, "[i]t must appear from the face of the instrument that what is covered by the reissue was intended to have been covered and secured by the original." *U.S. Indus. Chems., Inc. v. Carbide & Carbon Chems. Corp.*, 315 U.S. 668, 676 (1942). Furthermore, "it is not enough that an invention might have been claimed in the original patent because it was suggested or indicated in the specification." *Id.* In other words, the original patent "must clearly and unequivocally disclose the newly claimed invention as a separate invention." *Antares Pharma, Inc. v. Medac Pharma Inc.*, 771 F.3d 1354, 1362 (Fed. Cir. 2014).

This situation is also somewhat analogous to the Federal Circuit decision in *Antares*. In *Antares*, the original patent claims were drawn to various embodiments of a jet injection device that specify, for example, the exact depth the needle assist plunges to, the force at which the medicant is expelled, and the gauge of the needle. (*Antares* at 1356). In reissue, patentee broadened the claims to cover embodiments of injection devices with particular combinations of safety features. (*Id.*) The Federal Circuit determined that the new claims did not comply with the original patent requirement of section § 251 because the face of the patent (*i.e.*, via the

abstract, summary of invention, specification and all disclosed embodiments) provides "'suggest[ions]' or 'indicat[ions]' of alternative inventions [that] are not sufficient to satisfy the original patent requirement of § 251." (*Id*. at 1363). The Court concluded that the specification did not clearly and unequivocally disclose the particular combinations of safety features claimed on reissue, separate from the jet injection invention, thus, the original patent requirement was violated by broadening the claims to the separate invention. (*Id*.).

In the instant case, it does not appear from the face of the original patent that Applicant intended to cover 1). a generic memory device 2.) without a substrate. The Title includes reference to "NAND." The Abstract mentions and focusses on "NAND." The Background section references "NAND." All the figures depict NAND wafers. The claims as filed and during prosecution were drawn to NAND wafers. Independent claims 24, 39, and 49 are missing the NAND wafer.

Similarly, the patent here does not clearly and unequivocally disclose any embodiment that includes other non-NAND memory wafers. Despite the fact that the '283 Patent has boilerplate language suggesting "such examples could also be applied to other devices, such as universal flash storage (UFS), solid state memory, Dynamic Random access memory (DRAM) or other such volatile or non-volatile memory," Examiner finds this statement is no more than mere suggestions and/or indications of a claimed invention and not a fully described invention, in order to satisfy the original patent requirement of § 251 (*i.e.*, "it is not enough that an invention might have been claimed in the original patent because it was suggested or indicated in the specification; *Indus Chems* at 676). Thus, to broaden the claims to permit such an embodiment runs afoul of the original patent requirement.

The paragraphs above focus on the requirement for NAND wafers, but a similar argument exists for requiring the claimed device to have a substrate and its coupling in each independent claim. The Abstract, Background, and original claims all contain a substrate and some electrically conductive coupling to the substrate. No embodiments eliminate the substrate nor its coupling.

Claims 25-38, 40-48, and 50 are similarly rejected based on their dependency from independent claims 24, 39, and 49, respectively.

XII. Claim Rejections – 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

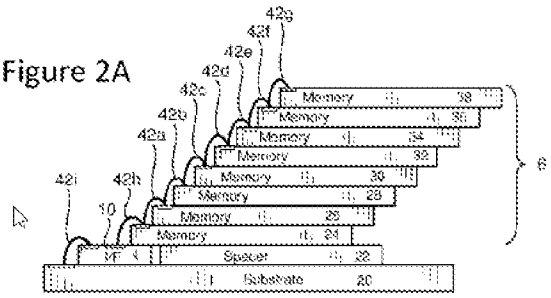
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

A. Claims **1, 2, 5-8, 10-13, 18-29, 34-37, 39-44, and 49** are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over **US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra")** in view of **US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano")**.

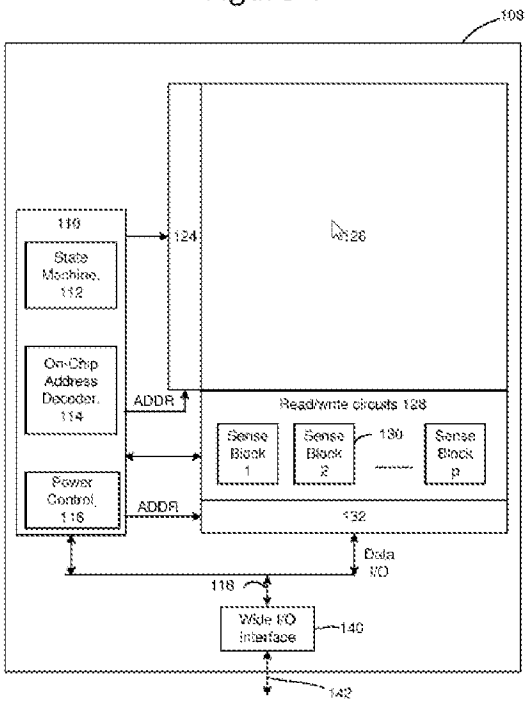
As to claim 1, Ramachandra teaches a microelectronic package, comprising: a substrate (#20 in Fig. 2 and in ¶ [0018]) having first and second opposite surfaces (bottom and top surfaces) each extending in first and second orthogonal directions (into the page and left to right); a NAND wafer (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]) having a memory storage array (#126 in Fig. 2 and in ¶ [0029]) therein, the NAND wafer having element contacts (#66 in Fig. 3 and in ¶ [0025]) electrically connected with electrically conductive structure of the substrate (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]), the NAND wafer being coupled to the first surface of the substrate (via spacer #22 in Fig. 2A or without spacer in Fig. 2D and in ¶ [0018], [0024]); a bitline driver (#132 and/or #128 in Fig. 4 and in ¶ [0030, [0032], [0039]) configured to function as a bitline driver for the NAND wafer, the bitline driver being elongated along the first direction and mounted to a front surface of the NAND wafer (Fig. 4 showing #132 and/or #128 elongated in the first direction); and a wordline driver (#124 and/or #110 in Fig. 4 and in ¶ [0030, [0031], [0039]) configured to function as a wordline driver for the NAND wafer, the wordline driver being elongated along the second direction and mounted to the front surface of the NAND wafer (Fig. 4 showing #124 and/or #110 being elongated in the second direction), wherein front surfaces of the bitline driver and the wordline driver are arranged in a single common plane and are entirely contained within an outer periphery of the front surface of the NAND wafer (Everything in the plane of and contained within the rectangle #108 in Fig. 4, #108 is a memory die representing those in Fig. 2, ¶ [0028]).

Figure 2A



Ramachandra Fig. 2A

Figure 4



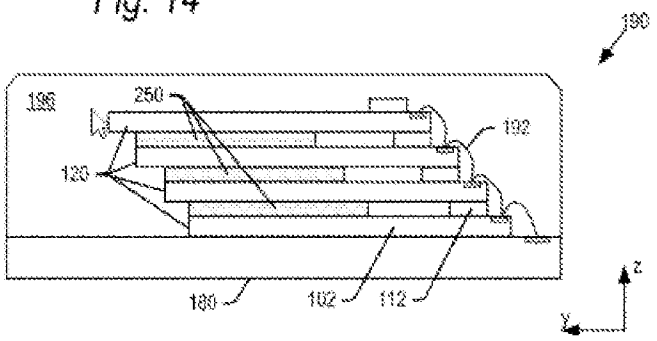
Ramachandra Fig. 4

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits can be mounted on the NAND wafer as chiplets.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as chiplets (#112 on #120 in Fig. 14). Hirano teaches the chips to contain

drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

Fig. 14



Hirano Fig. 14

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as chiplets as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

As to claim 2, both the layouts of Ramachandra (Fig. 4) and Hirano (Fig. 8) suggest general locations for a bitline driver chiplet and the wordline chiplet. They show bitline structure along a first peripheral edge of the NAND wafer and wordline structure perpendicular to the bitline structure. While neither reference specifically discloses the wordline driver chiplet being disposed along a centerline of the front surface that bisects the first peripheral edge, such a placement or orientation would have been obvious to one of ordinary skill in the art

since such a layout appears to be no more than a rearrangement of parts which would have been obvious to one of ordinary skill in the art based on a desired wiring layout of which would not have modified the operation of the device (MPEP 2144 VI).

As to claim 5, Ramachandra teaches a plurality of wire bonds (#42 in Fig. 2 and in ¶ [0021]) extending above the front surface of the NAND wafer, the plurality of wire bonds extending between the element contacts and substrate contacts at the first surface of the substrate (Fig. 2).

As to claim 6, Ramachandra teaches the NAND wafer is a first NAND wafer, the microelectronic package further comprising a plurality of NAND wafers including the first NAND wafer, the plurality of NAND wafers being arranged in a vertical stack and coupled to the first surface of the substrate (Fig. 2, stacked memory 24, 26, 28...).

As to claim 7, Ramachandra is silent about a device wherein the bitline driver chiplet is configured to function as a bitline driver that is shared by each of the plurality of NAND wafers, and the wordline driver chiplet is configured to function as a wordline driver that is shared by each of the plurality of NAND wafers.

However, Hirano teaches that a device wherein a plurality of NAND wafers can be driven by a driver on or near a first of the plurality of NAND wafers (Fig. 15, ¶ [0069]). Hirano discloses a device wherein each NAND wafer is driven by respective sets of drivers **or** a plurality of NAND wafers are driven by a single set of drivers, thus exemplifying art-recognized equivalent driver structure.

Therefore, because these two driver structures were art-recognized equivalents at the time the invention was made, a person of ordinary skill in the art would have found it obvious

to substitute respective sets of bitline and wordline driver chiplets in Ramachandra with a single set of bitline and wordline driver chiplets.

Moreover, the Examiner finds that simple substitution of one known element for another would obtain predictable results. That is, the substitution of one known element (respective sets of bitline and wordline drivers for each NAND wafer) for another (a single set of bitline and wordline driver chiplets controlling multiple NAND wafers) would have been obvious to one of ordinary skill in the art at the time of the invention since the substitution of multiple driver chiplet sets for a single driver chiplet set would have yielded predictable results, namely, driving the NAND wafers in the device while saving space and cost in the device.

As to claim 8, Ramachandra teaches comprising a plurality of wire bonds extending above the front surface of the first NAND wafer, the plurality of wire bonds extending between the element contacts of the first NAND wafer and substrate contacts at the first surface of the substrate, the plurality of wire bonds being configured to carry address information and data signals to each of the plurality of NAND wafers (#42a-i in Fig. 2 allowing connection between a controller and the wafers in ¶ [0021]-[0022]).

As to claim 10, Ramachandra teaches the bitline driver is a first bitline driver and the wordline driver is a first wordline driver, the microelectronic package further comprising a plurality of bitline drivers including the first bitline driver and a plurality of wordline drivers including the first wordline driver, each of the bitline drivers and each of the wordline driver being mounted to a corresponding one of the plurality of NAND wafers (Each of the NAND wafers of Fig. 2 having the structure of Fig. 4 as discussed in ¶ [0028]). Hirano teaches the drivers can be chiplets. The motivation to combine is the same as in claim 1.

As to claim 11, Ramachandra teaches a plurality of groups of wire bonds, each group of wire bonds extending above the front surface of a respective one of the NAND wafers (different groups and combinations shown throughout Fig. 2), each group of wire bonds extending between element contacts of the respective one of the NAND wafers and substrate contacts at the first surface of the substrate (Fig. 2). Examiner notes that this structure appears met by at least Fig. 2B which shows at least two groups (44a and 44c, or 44b and 44c). Further, Hirano also teaches different wire bond configurations for conducting signals such as Fig. 13 which shows two distinct groups (left and right #192) which extend from different wafers all the way to the substrate). Hirano also teaches wire bonds for signal transfer (¶ [0059]). It would have been obvious to one of ordinary skill in the art to use any of the layouts or similar layouts to those described in Ramachandra and Hirano since such a layout appears to be no more than a rearrangement of parts which would have been obvious to one of ordinary skill in the art based on a desired wiring layout of which would not have modified the operation of the device (MPEP 2144 VI).

As to claim 12, Ramachandra teaches a device wherein plurality of NAND wafers are arranged in a staircase configuration, such that each of the plurality of NAND wafers that is below the first NAND wafer is horizontally offset from the NAND wafer that is directly thereabove in the stack by an offset distance in either the first direction or the second direction (Fig. 2).

As to claim 13, Ramachandra teaches a plurality of groups of wire bonds, each group of wire bonds extending above the front surface of a respective one of the NAND wafers, element contacts of each of the plurality of NAND wafers that is below the first NAND wafer being

connected to element contacts of the NAND wafer that is directly thereabove in the stack by one of the groups of wire bonds (Fig. 2).

As to claim 18, Ramachandra teaches microelectronic assembly including the microelectronic package of claim 1, further comprising a circuit panel having panel contacts, wherein terminals at the second surface of the substrate (as interpreted in light of the 112 rejection above) are bonded to the panel contacts (¶ [0019] discussing the substrate electrically connected to a controller).

As to claim 19, Ramachandra teaches system comprising a microelectronic package according to claim 1 and one or more other electronic components electrically connected to the microelectronic package (¶ [0019] for connected to a host device or a controller).

As to claim 20, Ramachandra teaches a housing, the microelectronic package and the other electronic components being mounted to the housing (¶ [0019] for at least a molding compound to serve as a housing).

As to claim 21, Ramachandra teaches a microelectronic package, comprising: a substrate (#20 in Fig. 2 and in ¶ [0018]) having first and second opposite surfaces (bottom and top surfaces) each extending in first and second orthogonal directions (into the page and left to right); a plurality of microelectronic elements (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]) arranged in a vertical stack and coupled to the first surface of the substrate (via spacer #22 in Fig. 2A or without spacer in Fig. 2D and in ¶ [0018], [0024]); the microelectronic elements each having element contacts (#66 in Fig. 3 and in ¶ [0025]) electrically connected with electrically conductive structure of the substrate (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]); and a plurality of drivers (#132 and/or #128, (#124 and/or #110 in Fig. 4 and in ¶ [0030-0032],

[0039]) arranged within the vertical stack and coupled to the plurality of microelectronic elements, the drivers being alternatingly interleaved with the microelectronic elements within the vertical stack such that at least one of the microelectronic elements is directly coupled to multiple drivers, circuitry of each of the drivers being electrically connected with circuitry of at least one of the microelectronic elements, wherein front surfaces of each of the drivers are entirely contained within an outer periphery of the front surfaces of each of the microelectronic elements (Everything in the plane of and contained within the rectangle #108 in Fig. 4, #108 is a memory die representing those in Fig. 2, ¶ [0028]).

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits/drivers can be mounted on the NAND wafer (microelectronic elements) as chiplets.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as chiplets. Hirano teaches the chips to contain drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]). Finally, Hirano even teaches that the chiplets can be interleaved between the NAND wafers (microelectronic elements) in Fig. 14.

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as chiplets as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

As to claim 22, the rejection of claim 21 addresses how the plurality of drivers in Ramachandra can be replaced with multiple chiplets. The motivation to combine is the same as in claim 21.

As to claim 23, Ramachandra teaches a method of assembling a microelectronic package, the method comprising: providing a substrate (#20 in Fig. 2 and in ¶ [0018]) having first and second opposite surfaces (bottom and top surfaces) each extending in first and second orthogonal directions (into the page and left to right);; coupling a NAND wafer (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]) to the first surface of the substrate, the NAND wafer having a memory storage array (#126 in Fig. 2 and in ¶ [0029]) therein; electrically connecting element contacts (#66 in Fig. 3 and in ¶ [0025]) of the NAND wafer with electrically conductive structure of the substrate (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]); mounting a bitline driver (#132 and/or #128 in Fig. 4 and in ¶ [0030, [0032], [0039]) to a front surface of the NAND wafer, the bitline driver configured to function as a bitline driver for the NAND wafer, the bitline driver being elongated along the first direction (Fig. 4 showing #132 and/or #128 elongated in the first direction); and mounting a wordline driver (#124 and/or #110 in Fig. 4 and in ¶ [0030, [0031], [0039]) to the front surface of the NAND wafer, the wordline driver configured to function as a wordline driver for the NAND wafer, the wordline driver being elongated along the second direction (Fig. 4 showing #124 and/or #110 being elongated in the

second direction), wherein front surfaces of the bitline driver and the wordline driver are arranged in a single common plane and are entirely contained within an outer periphery of the front surface of the NAND wafer (Everything in the plane of and contained within the rectangle #108 in Fig. 4, #108 is a memory die representing those in Fig. 2, ¶ [0028]).

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits can be mounted on the NAND wafer as chiplets.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as chiplets. Hirano teaches the chips to contain drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as chiplets as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

As to claim 24, Ramachandra teaches a device structure comprising: a memory device comprising: a first die (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]) comprising a memory

cell array (#126 in Fig. 2 and in ¶ [0029]) and bitlines and wordlines for the memory cell array (¶ [0031]); and a plurality of drivers disposed on a surface of the first die, the plurality of drivers comprising a wordline driver (#124 and/or #110 in Fig. 4 and in ¶ [0030, [0031], [0039]) and a bitline driver (#132 and/or #128 in Fig. 4 and in ¶ [0030, [0032], [0039]) disposed laterally adjacent to the wordline driver.

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits can be mounted on the NAND wafer as dies.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as dies. Hirano teaches the chips to contain drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as dies as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

As to claim 25, Ramachandra teaches the memory device is disposed on and electrically

connected (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]) to a package substrate (#20 in Fig. 2 and in ¶ [0018]).

As to claim 26, Ramachandra teaches a plurality of wire bonds (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]) extending between a plurality of conductive elements (#66 in Fig. 3 and in ¶ [0025]) in the surface of the first die to the package substrate to electrically connect the first die to the package substrate.

As to claim 27, Ramachandra teaches the first die comprises opposing first edges that extend in a first direction and opposing second edges that extend in a second direction orthogonal to the first direction (into the page and left to right); the plurality of conductive elements are disposed proximate to one of the first edges (Fig. 3); and the bitline driver is elongated in the first direction and is disposed adjacent to the plurality of wire bonds (Fig. 4). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 24.

As to claim 28, Ramachandra teaches the wordline driver is elongated in the second direction (Fig. 4 showing #124 and/or #110 being elongated in the second direction). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 24.

As to claim 29, Ramachandra teaches the wordline driver is disposed centrally between the opposing second edges (Fig. 4, located at least not on the edge). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 24. The Applicant's use of the term "centrally" is broader than similar limitations in claim 2. If the reviewing party finds "centrally" to mean along a centerline of the front surface that bisects the first edges (Claim 2), neither reference specifically discloses the wordline driver die being disposed along a centerline of the front surface that bisects the first edges. However, such a placement or orientation

would have been obvious to one of ordinary skill in the art since such a layout appears to be no more than a rearrangement of parts which would have been obvious to one of ordinary skill in the art based on a desired wiring layout of which would not have modified the operation of the device (MPEP 2144 VI).

As to claim 34, Ramachandra teaches a device structure comprising a stack of memory devices each according to the first die of claim 24 (Fig. 2). Hirano also teaches that the dies can be interleaved between the NAND wafers (microelectronic elements) in Fig. 14. The motivation to combine is the same as in claim 24.

As to claim 35, Ramachandra teaches the stack of memory devices are vertically aligned (Fig. 2, having at least part of the memory devices above one another, see specifically Fig. 2C for showing at least two devices completely aligned in the vertical direction).

As to claim 36, Ramachandra teaches each memory device is offset in a horizontal direction relative to an adjacent memory device disposed therebelow (Fig. 2).

As to claim 37, Ramachandra teaches wire bonds extend between conductive elements of at least two vertically adjacent memory devices (Fig. 2).

As to claim 39, Ramachandra teaches a device structure comprising: a memory device comprising: a die stack comprising a plurality of first die (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]), each first die comprising a memory cell array (#126 in Fig. 2 and in ¶ [0029]) and bitlines and wordlines for the memory cell array (¶ [0031]); and a plurality of drivers disposed on a surface of the die stack, the plurality of second drivers comprising a wordline driver (#124 and/or #110 in Fig. 4 and in ¶ [0030, [0031], [0039]) and a bitline driver (#132 and/or #128 in Fig. 4 and in ¶ [0030, [0032], [0039]) disposed laterally adjacent to the wordline driver.

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits can be mounted on the NAND wafer as dies.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as dies. Hirano teaches the chips to contain drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as dies as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

As to claim 40, Ramachandra teaches the memory device is disposed on and electrically connected (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]) to a package substrate (#20 in Fig. 2 and in ¶ [0018]).

As to claim 41, Ramachandra teaches a plurality of wire bonds (via #42 or #44 in Fig. 2 and 3 and in ¶ [0021-0022]) extending between a plurality of conductive elements (#66 in Fig. 3 and in ¶ [0025]) in the surface of the first die to the package substrate to electrically connect

the first die to the package substrate.

As to claim 42, Ramachandra teaches the first die comprises opposing first edges that extend in a first direction and opposing second edges that extend in a second direction orthogonal to the first direction (into the page and left to right); the plurality of conductive elements are disposed proximate to one of the first edges (Fig. 3); and the bitline driver is elongated in the first direction and is disposed adjacent to the plurality of wire bonds (Fig. 4). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 39.

As to claim 43, Ramachandra teaches the wordline driver is elongated in the second direction (Fig. 4 showing #124 and/or #110 being elongated in the second direction). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 39.

As to claim 43, Ramachandra teaches the wordline driver is disposed centrally between the opposing second edges (Fig. 4, located at least not on the edge). Hirano teaches the drivers to be dies. The motivation to combine is the same as in claim 24. If the reviewing party finds "centrally" to mean along a centerline of the front surface that bisects the first edges (Claim 2), neither reference specifically discloses the wordline driver die being disposed along a centerline of the front surface that bisects the first edges. However, such a placement or orientation would have been obvious to one of ordinary skill in the art since such a layout appears to be no more than a rearrangement of parts which would have been obvious to one of ordinary skill in the art based on a desired wiring layout of which would not have modified the operation of the device (MPEP 2144 VI).

As to claim 49, Ramachandra teaches a device structure comprising: a memory device comprising: a first die (#24 in Fig. 2 and in ¶ [0020], "NAND" in [0029]) comprising a memory

cell array (#126 in Fig. 2 and in ¶ [0029]) and bitlines and wordlines for the memory cell array (¶ [0031]); and a plurality of drivers disposed on a surface of the first die, the plurality of drivers comprising a wordline driver (#124 and/or #110 in Fig. 4 and in ¶ [0030, [0031], [0039]) and a bitline driver (#132 and/or #128 in Fig. 4 and in ¶ [0030, [0032], [0039]) disposed laterally adjacent to the wordline driver (Fig. 4).

Ramachandra is clear to teach that the mounting layout of Fig. 4 can be configured such that one or more components alone or in combination can be thought of as particular control circuits (¶ [0039]). However, Ramachandra does not specify that respective control circuits can be mounted on the NAND wafer as chiplets.

In the same field or endeavor, Hirano teaches mounting memory control circuitry on top of NAND wafers as chiplets. Hirano teaches the chips to contain drivers for at least word line layers [0048]) in one chip and another chip with drivers to perform tasks such as controlling and allocating memory (¶ [0051]). Finally, Hirano even teaches that other control structure on the NAND wafer could also be moved between the different dies (¶ [0049]). Hirano teaches removing the logic circuit from the first die (NAND wafer itself) to free up valuable space for additional memory cells (on the NAND wafer). It also allows for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

It would have been obvious to one of ordinary skill in the art to form the drivers of Ramachandra as chiplets as taught by Hirano in order to free up valuable space for additional memory cells (on the NAND wafer) and allow for customized and optimized fabrication processes for the separate wafers (¶ [0032]-[0033]).

B. Claims **3, 9, 30, 31, 45, 46, 50** are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over **US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra")** and **US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano")** as applied to claims 1, 7, 24, 39, and 49 above, and further in view of **US 8,399,974 B1 to Huneke ("Huneke")**.

As to claims 3, 9, 30, 31, 45, 46 and 50, Ramachandra and Hirano are both silent about the chiplets/dies being directly bonded without the use of an intervening adhesive by hybrid bonding.

However, in the same field or endeavor, Huneke teaches stacked memory dies which are attached using a molecular bonding process to produce an essentially zero bond-line between the bonded die (Fig. 4, col. 1 ln. 18-20) in the interest of producing more compact electrical components (col. 2, ln. 30-40). Avoiding adhesive also avoids problems like unwanted adhesive paste flowing (col. 2, ln. 5). Huneke teaches forming a covalent bond between surfaces where the final product is essentially one integral structure (col. 5, ln. 56 – col. 6 ln. 4). Examiner notes that this covalent bond is the primary bond in hybrid bonding.

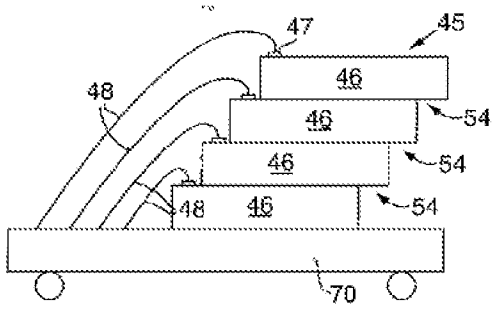


FIG. 4

Huneke Fig. 4

It would have been obvious to one of ordinary skill in the art to directly bond the chiplets/dies of Ramachandra and Hirano without the use of an intervening adhesive by hybrid

bonding as taught by Huneke in order to avoid the known problems with adhesive and produce an essentially zero bond-line between the bonded die in the interest of producing more compact electrical components.

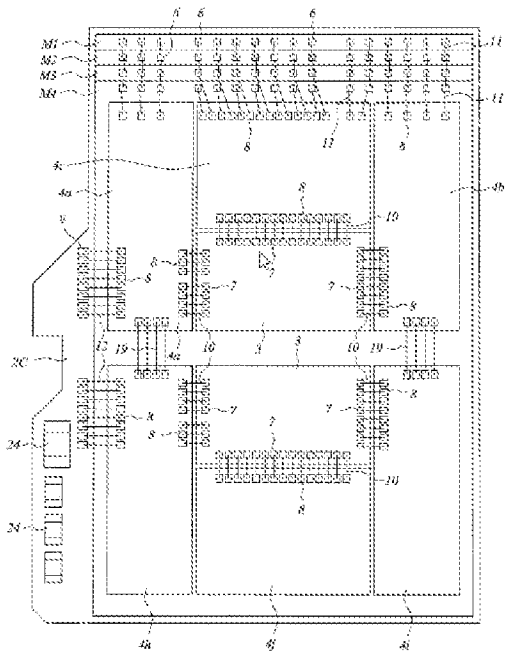
C. Claim **4** is rejected under pre-AIA 35 U.S.C. 103(a) as obvious over **US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra")** and **US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano")** as applied to claim 1 above, and further in view of **US Pub. No. 2009/0200680 A1 to Shinohara et al. ("Shinohara")**.

As to claim 4, Ramachandra and Hirano teach the bitline driver chiplet is a first bitline driver chiplet and the wordline driver chiplet is a first wordline driver chiplet, as well as their orientation while being mounted to the front surface of the NAND wafer (see rejection of claim 1 above). Ramachandra and Hirano are silent about the microelectronic package further comprising a plurality of bitline driver chiplets including the first bitline driver chiplet and a plurality of wordline driver chiplets including the first wordline driver chiplet, each of the bitline driver chiplets being spaced apart from one another, and each of the wordline driver chiplets being spaced apart from one another.

However, in the same field or endeavor, Shinohara teaches the use of multiple control chiplets mounted on top of the memory wafer (#3 in Fig. 39 and 40, note also multiple interposers #4). Shinohara teaches the use of extra chiplets spaced from one another in order to prevent the decrease in access rate between memory chips and the controller chip (¶ [0194]). Shinohara recognizes a problem with access rate when using multiple memory chips and solves it by multiplying the driver chips. Thus, it would have been obvious to one of

ordinary skill in the art to utilize a plurality of bitline and wordline driver chiplets in the device of Ramachandra and Hirano as taught by Shinohara in order to maintain access rate when stacking multiple memory chips together. Finally for any placement or orientation limitation deemed not to be met above, such a placement or orientation would have been obvious to one of ordinary skill in the art since such a layout appears to be no more than a rearrangement of parts which would have been obvious to one of ordinary skill in the art based on a desired wiring layout of which would not have modified the operation of the device (MPEP 2144 VI).

FIG. 40



Shinohara Fig. 40

D. Claims **14 and 15** are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over **US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra")** and **US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano")** as applied to claim 6 above, and further in view of **US Pub. No. 2008/0122064 A1 to Itoh et al. ("Itoh")**.

As to claim 14, Ramachandra teaches a plurality of NAND wafers are arranged in a staircase configuration, such that each of the plurality of NAND wafers that is below the first NAND wafer is horizontally offset from the NAND wafer that is directly thereabove in the stack by a first offset distance in the first direction (Fig. 2). Ramachandra and Hirano are silent about the NAND wafers also being offset by a second offset distance in the second direction.

However, in the same field or endeavor, Itoh teaches a similar staircase memory stack wherein the subsequent memory chips are offset by both a first and a second distance (Fig. 3). Itoh teaches this structure in order to allow for easier or optimal wiring. In particular, it allows power supply pads to be diagonally placed in order to avoid a reduction in performance due to internal wiring resistance. It also suppresses an increase in ground voltage (¶ [0067]).

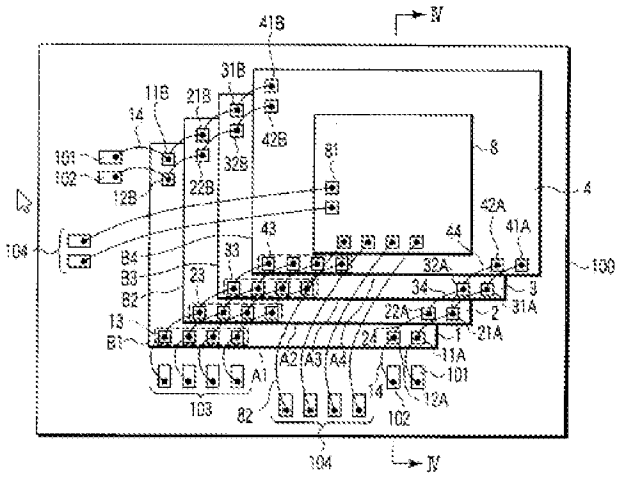


FIG. 3

Itoh Fig. 3

It would have been obvious to one of ordinary skill in the art to form the memory chip staircase of Ramachandra in view of Hirano to be offset in both a first and second distance as taught by Itoh in order to avoid a reduction in performance due to internal wiring resistance as well as suppress an increase in ground voltage in the staircase.

As to claim 15, Ramachandra teaches a plurality of groups of wire bonds, each group of wire bonds extending above the front surface of a respective one of the NAND wafers, element contacts of each of the plurality of NAND wafers that is below the first NAND wafer being connected to element contacts of the NAND wafer that is directly thereabove in the stack by one of the groups of wire bonds, each group of wire bonds having a first subset that extends over a first edge of the respective one of the NAND wafers (Fig. 2 and 3 showing multiple groups of wire bonds). Itoh teaches a second subset that extends over a second edge of the respective one of the NAND wafers adjacent to the first edge (Fig. 3 showing two subsets of wire bonds). The motivation to combine is the same as in claim 14.

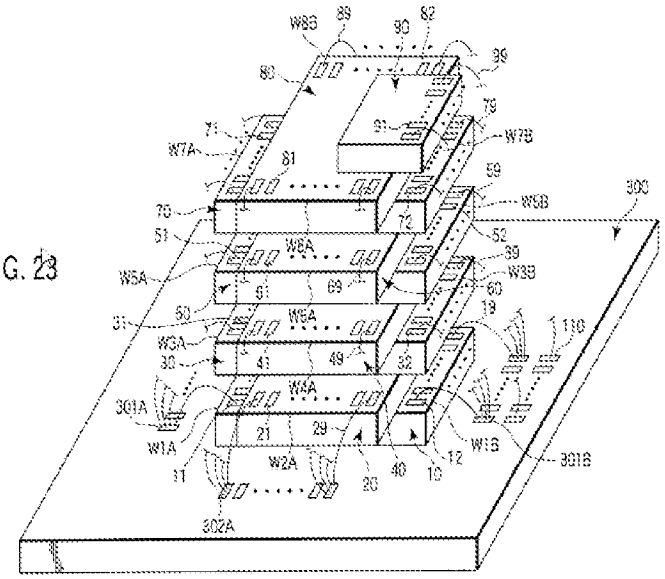
E. Claims **16, 17, 32, 33, 38, 47 and 48** are rejected under pre-AIA 35 U.S.C. 103(a) as obvious over **US. Pub. No. 2018/0102344 A1 to Ramachandra et al. ("Ramachandra")** and **US. Pub. No. 2019/0341375 A1 to Hirano et al. ("Hirano")** as applied to claims 6 and 34 above, and further in view of **US Pub. No. 2008/0157393 A1 to Kodama et al. ("Kodama")**.

As to claim 16, Ramachandra and Hirano teach NAND wafers but are silent about the plurality of NAND wafers being arranged in an alternating orthogonal configuration, such that long sides of each of the plurality of NAND wafers that is below the first NAND wafer are rotated 90 degrees relative to long sides of the NAND wafer that is directly thereabove in the

stack.

However, in the same field or endeavor, Kodama teaches the plurality of NAND wafers are arranged in an alternating orthogonal configuration, such that long sides of each of the plurality of NAND wafers that is below the first NAND wafer are rotated 90 degrees relative to long sides of the NAND wafer that is directly thereabove in the stack (Fig. 23-25, ¶ [0179]-[0205]). Kodama teaches this configuration in order to secure space in the direction of thickness for wire bonding of the underlying semiconductor (¶ [0202]) and simplify the leading of board interconnections (¶ [0204]). It would have been obvious to one of ordinary skill in the art to stack the NAND wafers of Ramachandra in view of Hirano in a manner taught by Kodama in order to secure space in the direction of thickness for wire bonding of the underlying semiconductor (¶ [0202]) and simplify the leading of board interconnections (¶ [0204]).

FIG. 23



Kodama Fig. 23

As to claim 17, Kodama teaches a plurality of groups of wire bonds, each group of wire bonds extending above the front surface of a respective one of the NAND wafers, each group of

wire bonds extending between element contacts of the respective one of the NAND wafers and substrate contacts at the first surface of the substrate, each group of wire bonds having a first subset that extends over a first short edge of the respective one of the NAND wafers and a second subset that extends over a second edge of the respective one of the NAND wafers opposite from the first edge (Fig. 23-25 showing wire bonds coming off both short sides of each wafer). The motivation to combine is the same as in claim 16.

As to claims 32, 33, 47 and 48, Ramachandra and Hirano are silent about the memory device being a volatile memory device or DRAM.

However, in the same field or endeavor, Kodama teaches that the memory chips can be DRAM which is a type of volatile memory (¶ [0055]). Kodama teaches that the memory chips can be NAND (non-volatile) or DRAM (volatile) (¶ [0055]).

Therefore, because these memory wafers were art-recognized equivalents at the time the invention was made, a person of ordinary skill in the art would have found it obvious to substitute respective NAND wafer memory in Ramachandra with volatile or DRAM memory.

Moreover, the Examiner finds that simple substitution of one known element for another would obtain predictable results. That is, the substitution of one known element (NAND wafer) for another (volatile or DRAM memory) would have been obvious to one of ordinary skill in the art at the time of the invention since the substitution of NAND wafers for volatile or DRAM memory would have yielded predictable results, namely, providing an alternate means for memory storage in the device.

As to claim 38, Ramachandra and Hirano are silent about each memory device is disposed in an orthogonal orientation relative to an adjacent memory device disposed

thereabove or therebelow.

However, in the same field or endeavor, Kodama teaches each memory device is disposed in an orthogonal orientation relative to an adjacent memory device disposed thereabove or therebelow (Fig. 23-25, ¶ [0179]-[0205]). Kodama teaches this configuration in order to secure space in the direction of thickness for wire bonding of the underlying semiconductor (¶ [0202]) and simplify the leading of board interconnections (¶ [0204]). It would have been obvious to one of ordinary skill in the art to stack the NAND wafers of Ramachandra in view of Hirano in a manner taught by Kodama in order to secure space in the direction of thickness for wire bonding of the underlying semiconductor (¶ [0202]) and simplify the leading of board interconnections (¶ [0204]).

I. Conclusion

Applicant is respectfully reminded that any suggestions or examples of claim language provided by the Examiner are just that—suggestions or examples—and do not constitute a formal requirement mandated by the Examiner. To be especially clear, any suggestion or example provided in this Office Action (or in any future office action) does not constitute a formal requirement mandated by the Examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANDREW J COUGHLIN whose telephone number is (571)270-7813. The examiner can normally be reached M-F 9 am - 5 pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hetul Patel can be reached on (571) 272-4184. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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